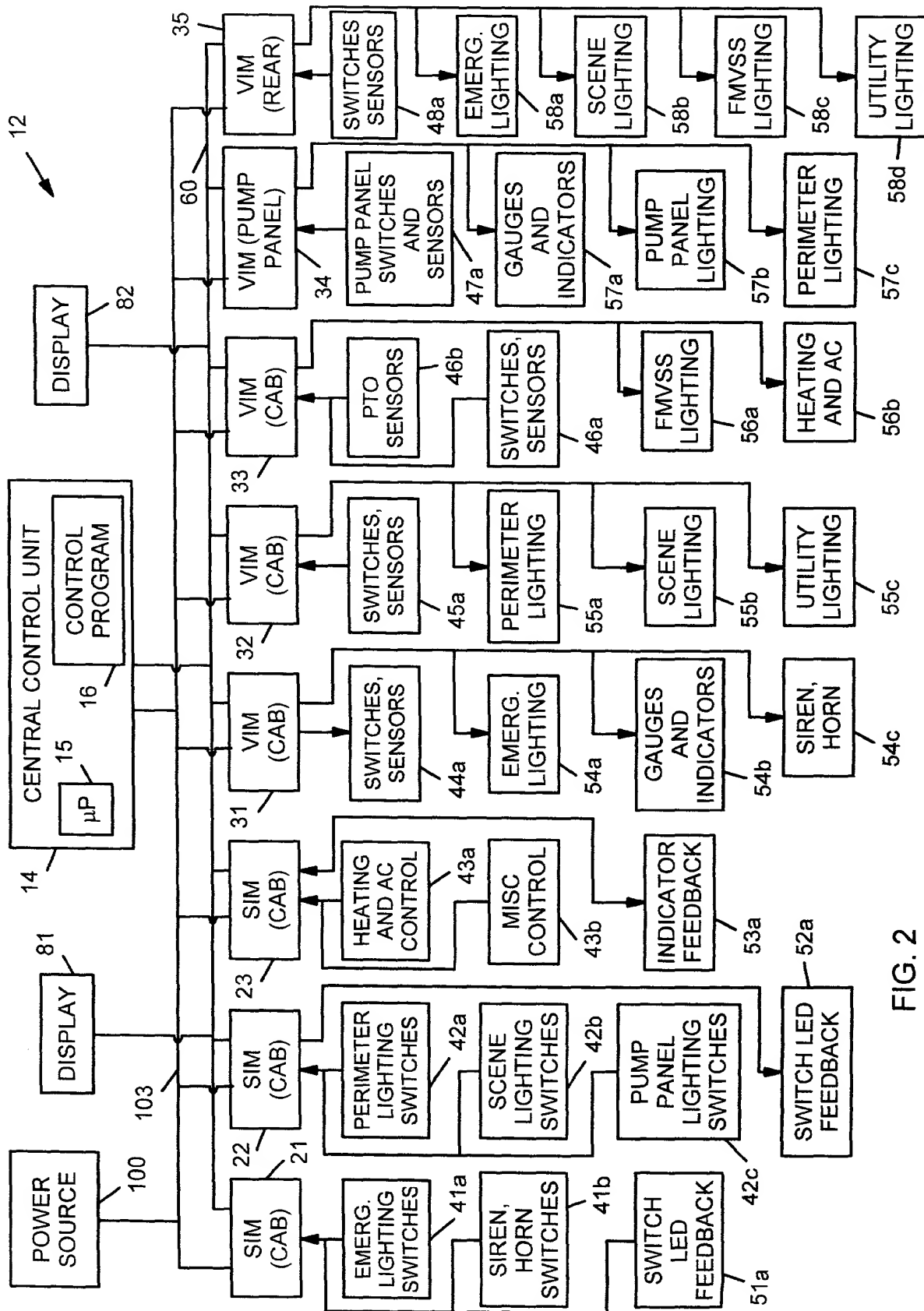


FIG. 1



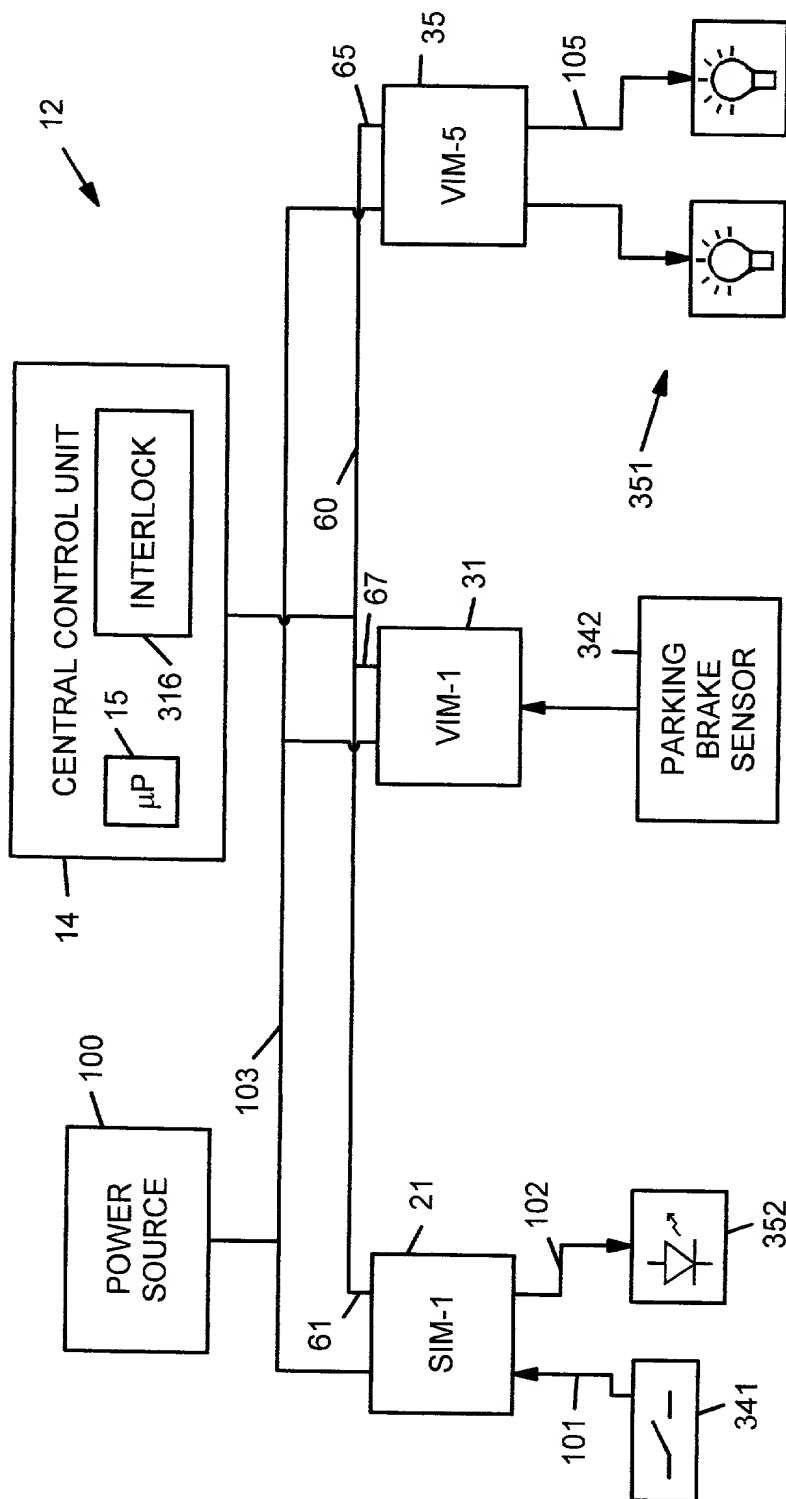


FIG. 3

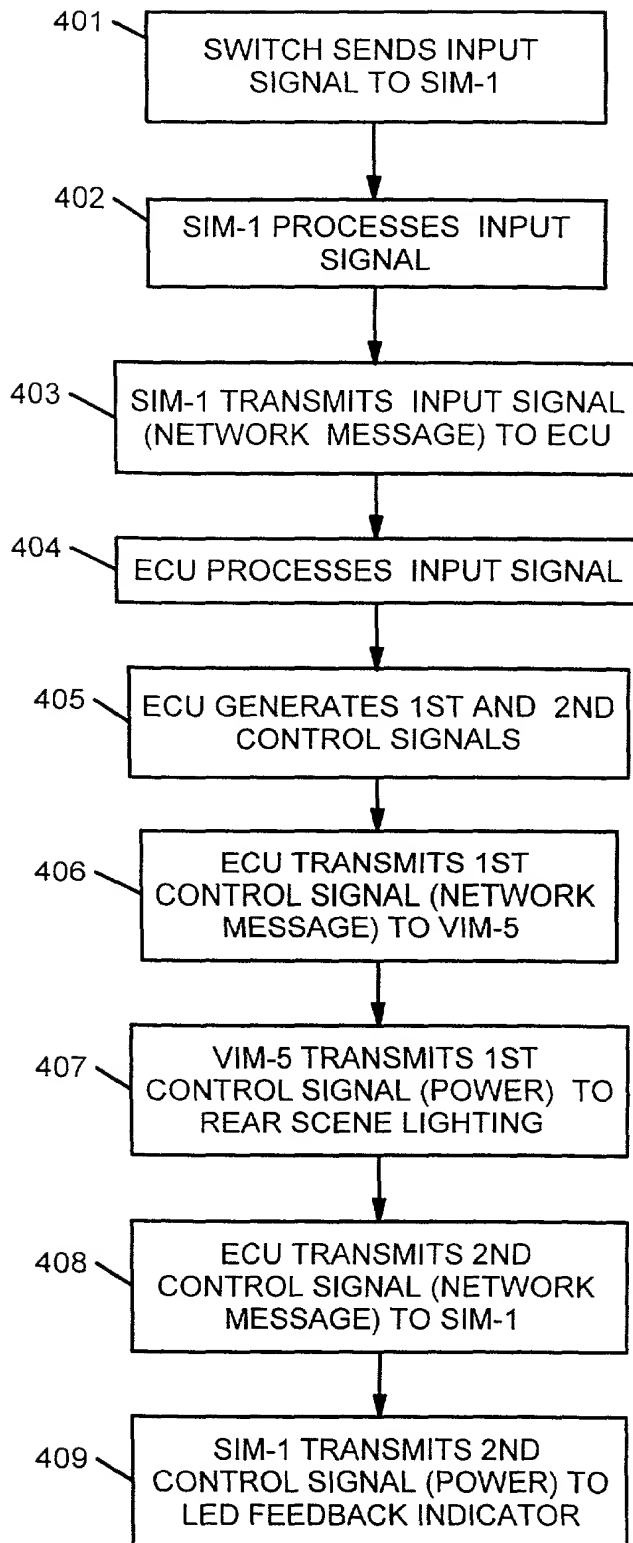


FIG. 4

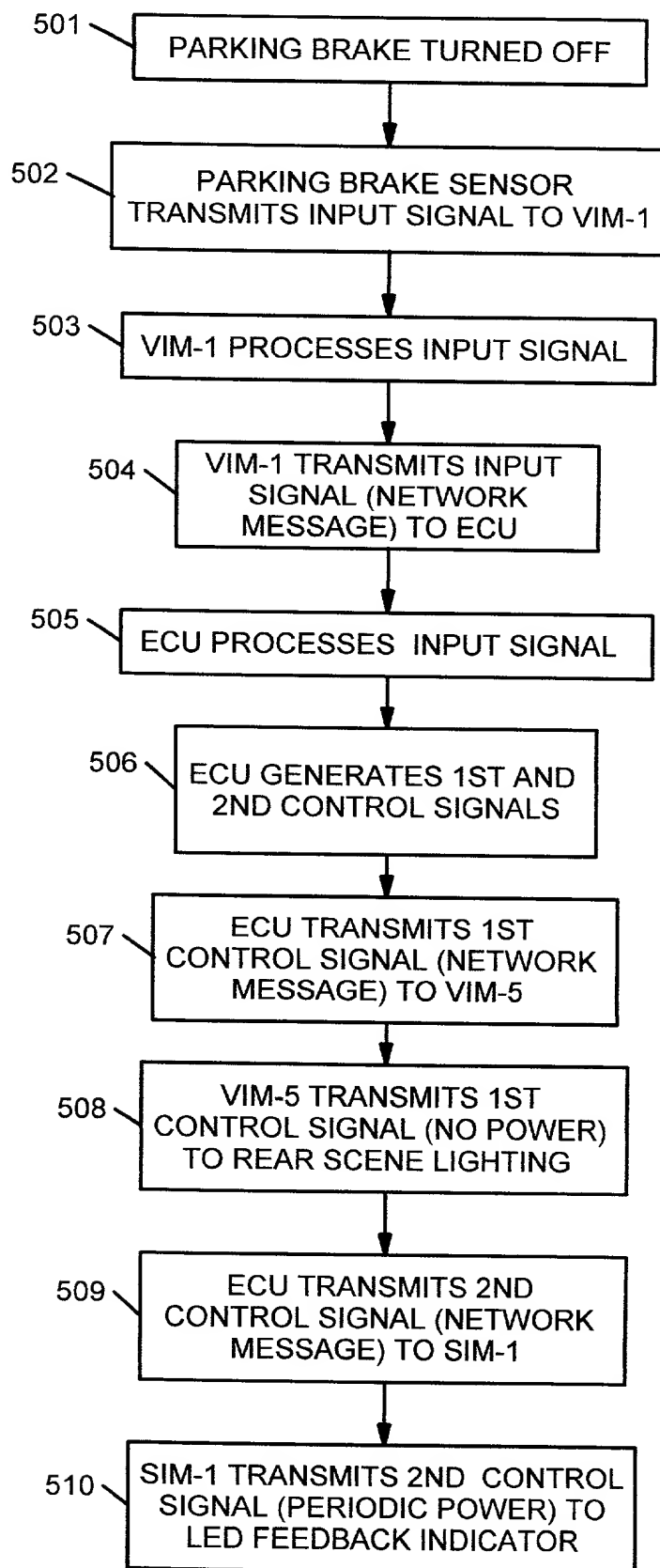


FIG. 5

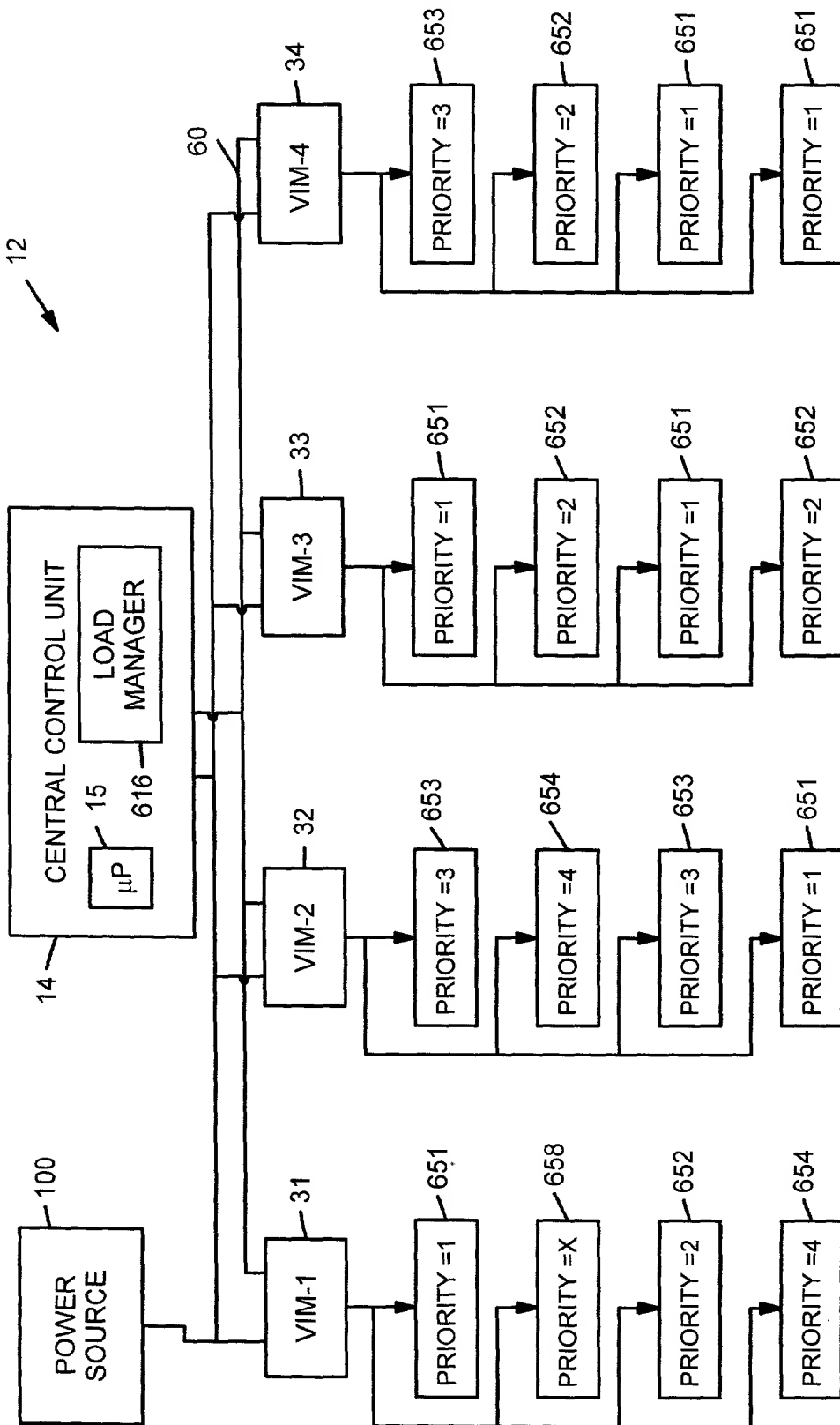
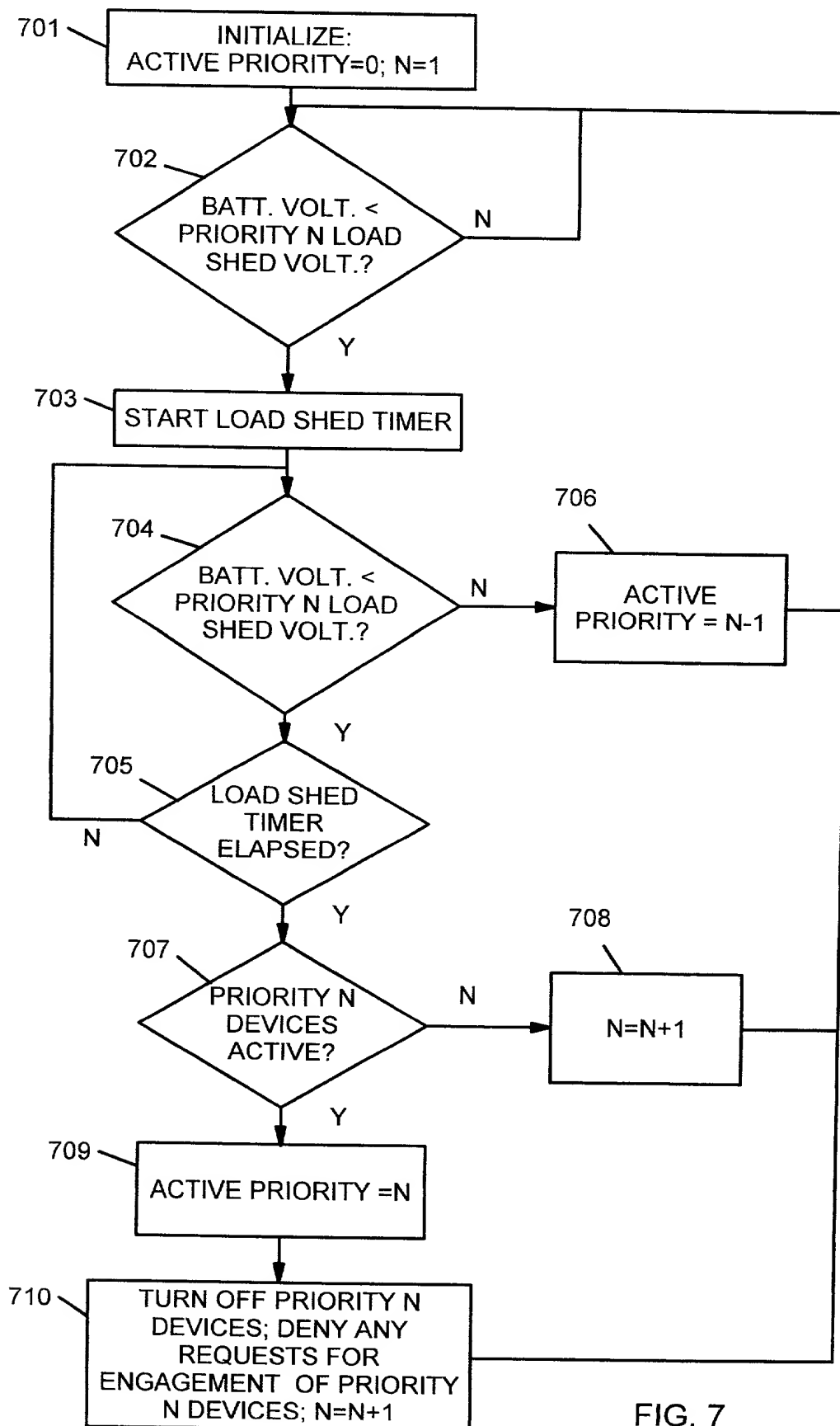


FIG. 6



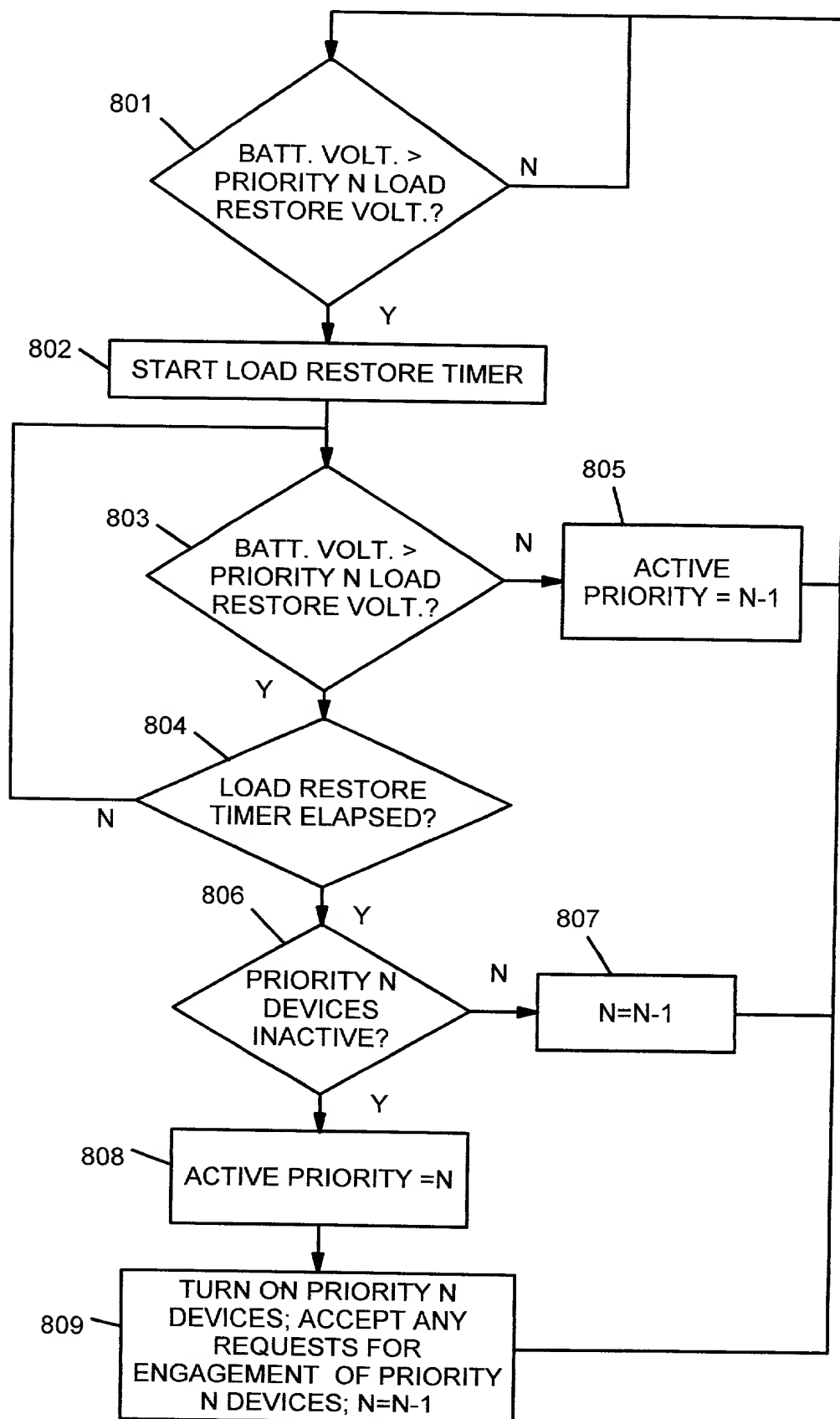


FIG. 8

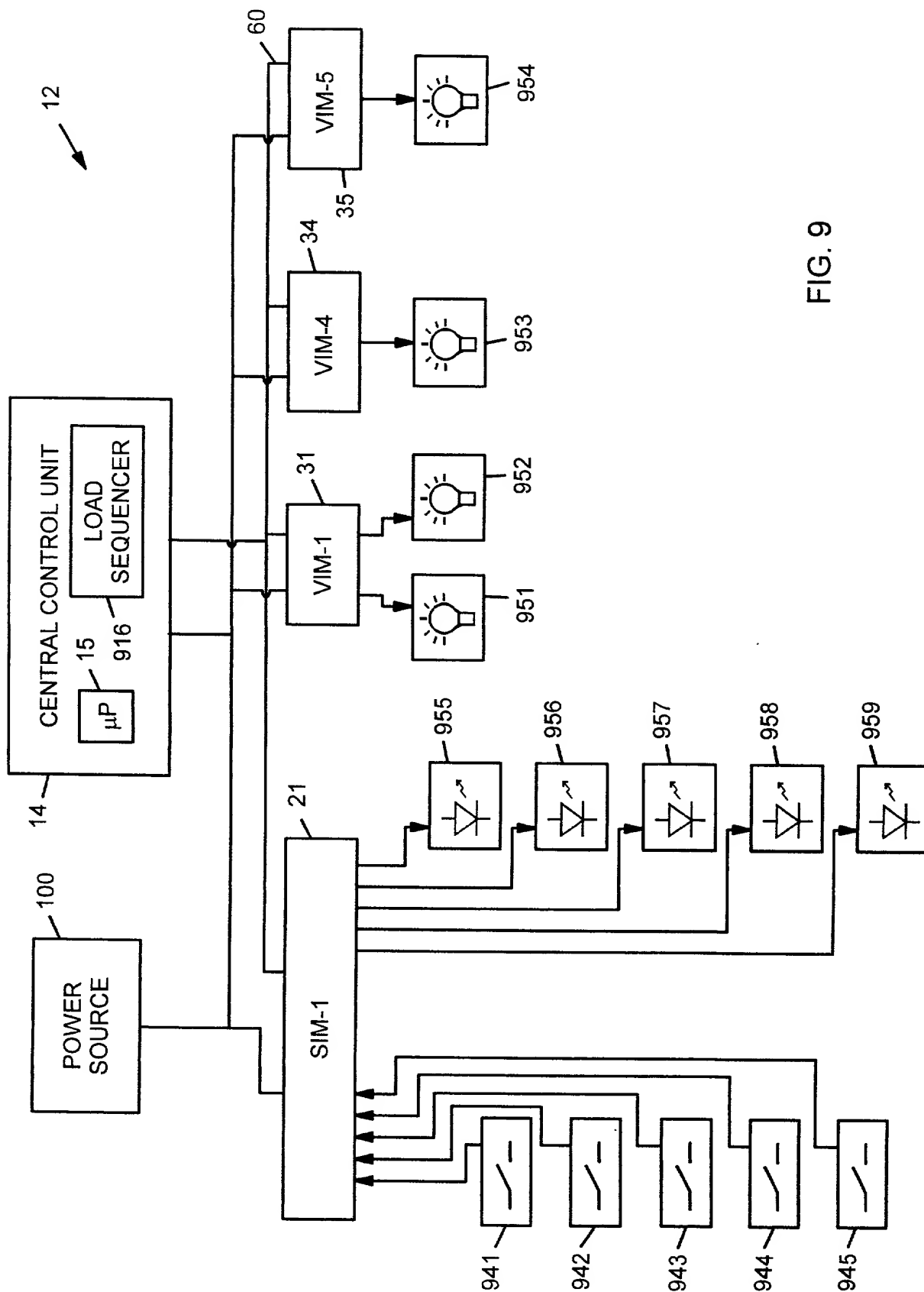


FIG. 9

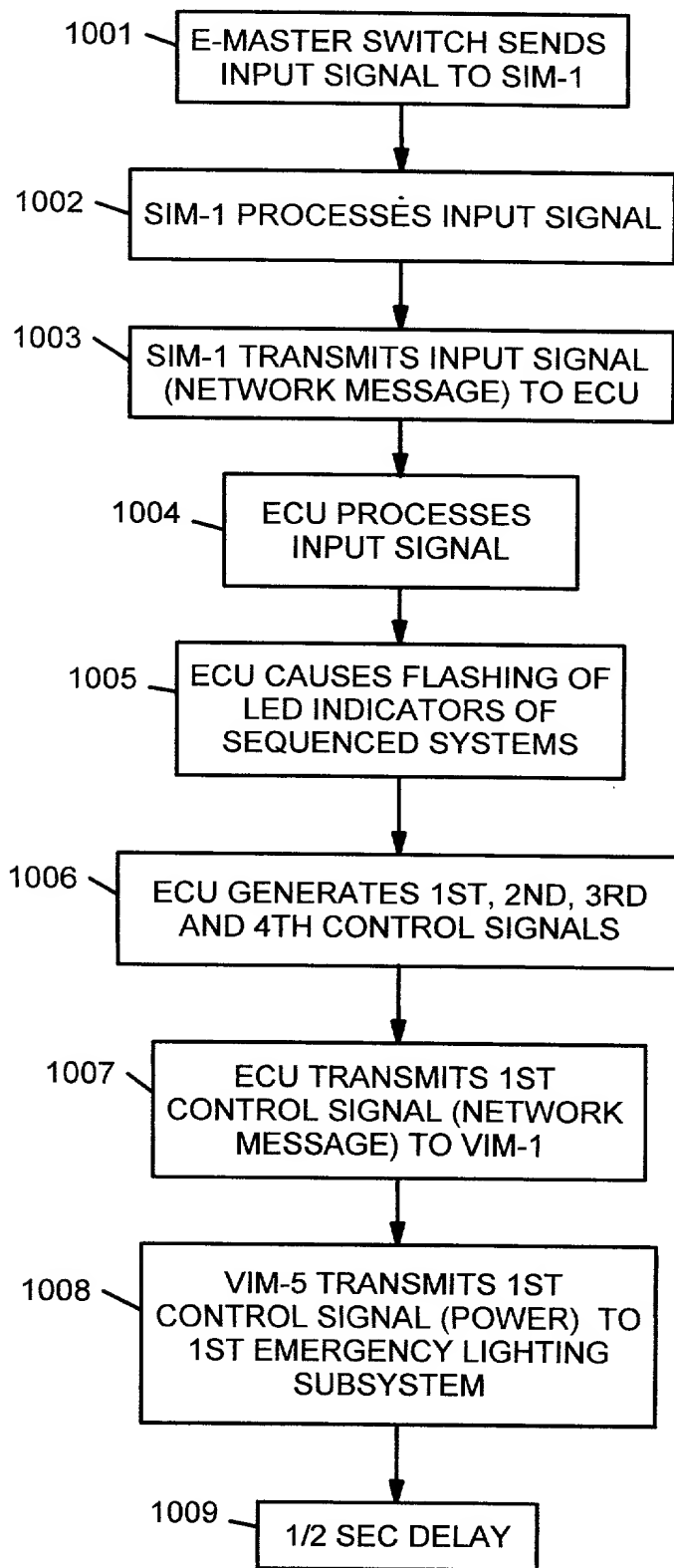


FIG. 10A

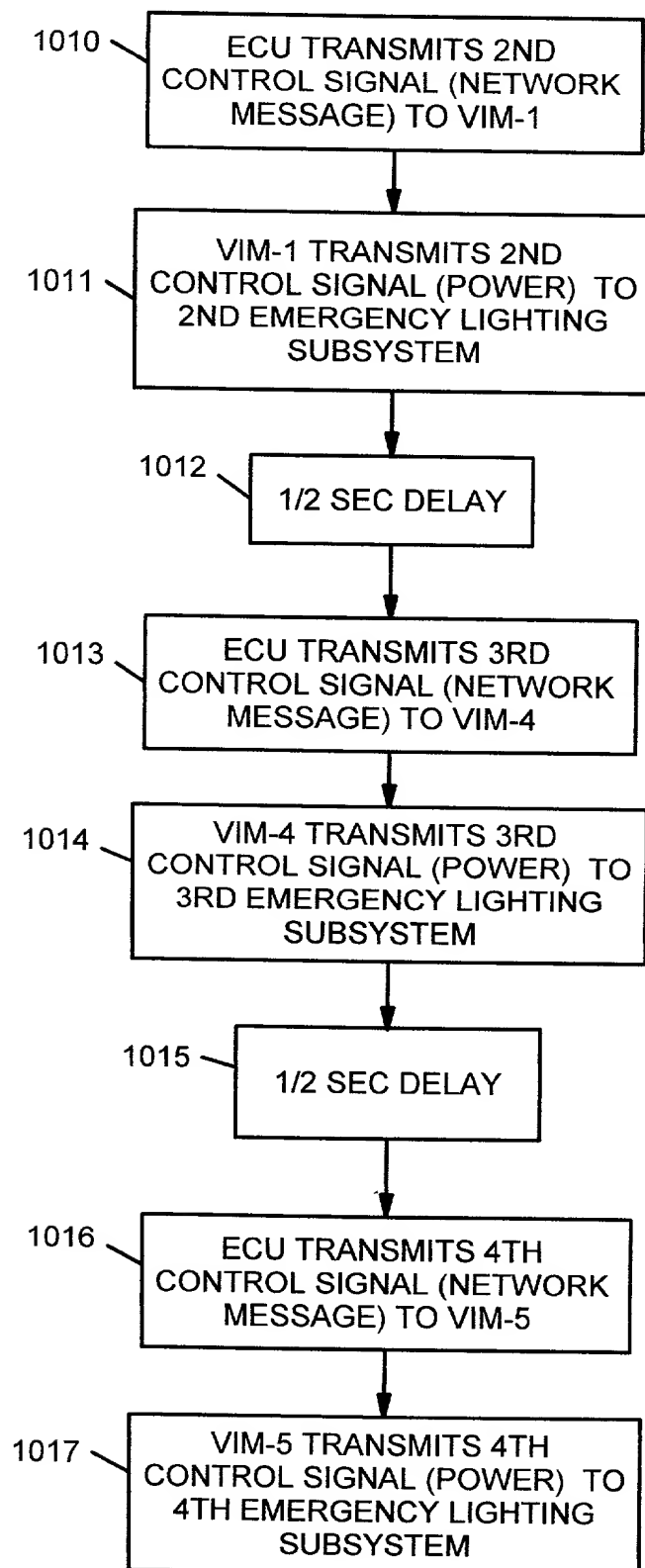


FIG. 10B

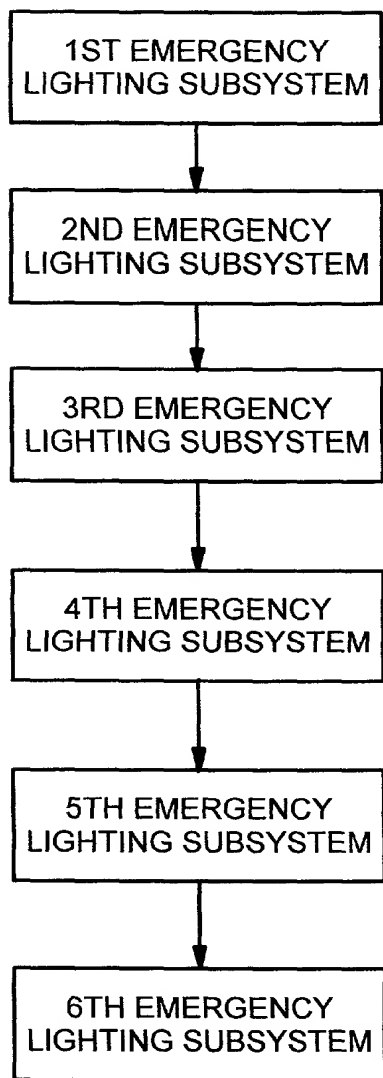


FIG. 11A

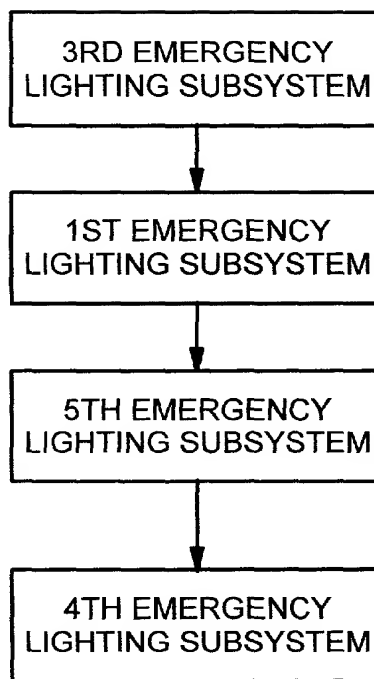


FIG. 11B

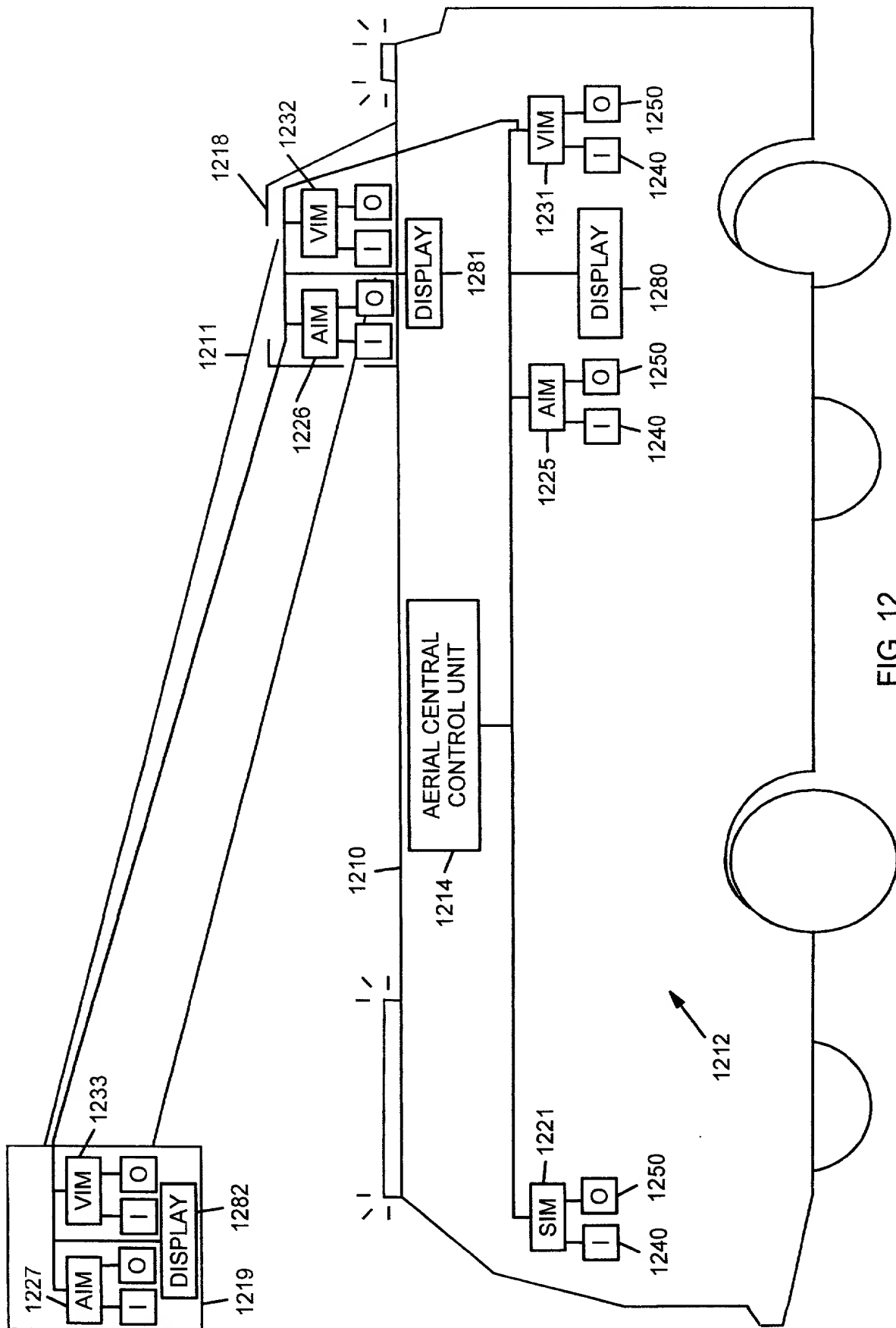


FIG. 12

FIG. 12

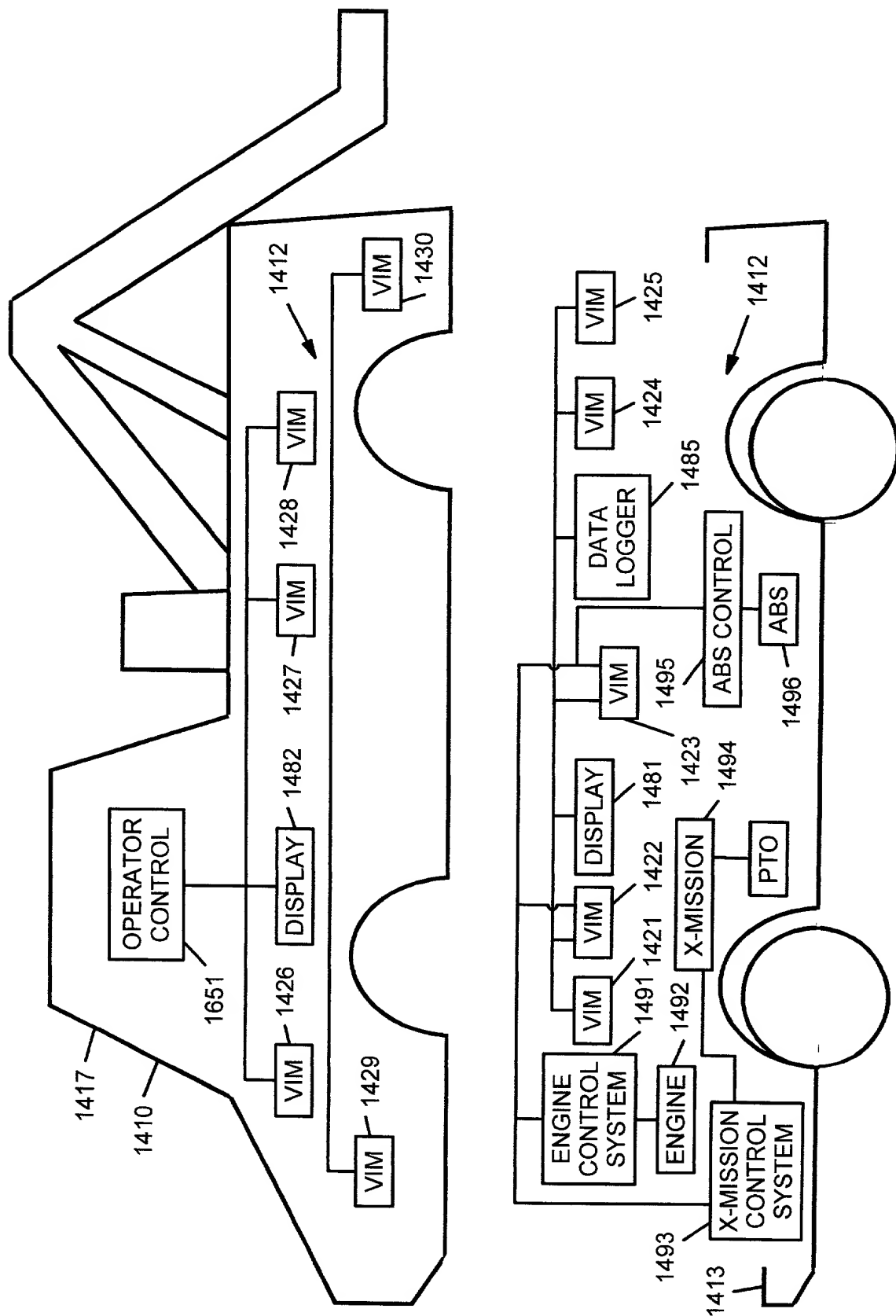


FIG. 14

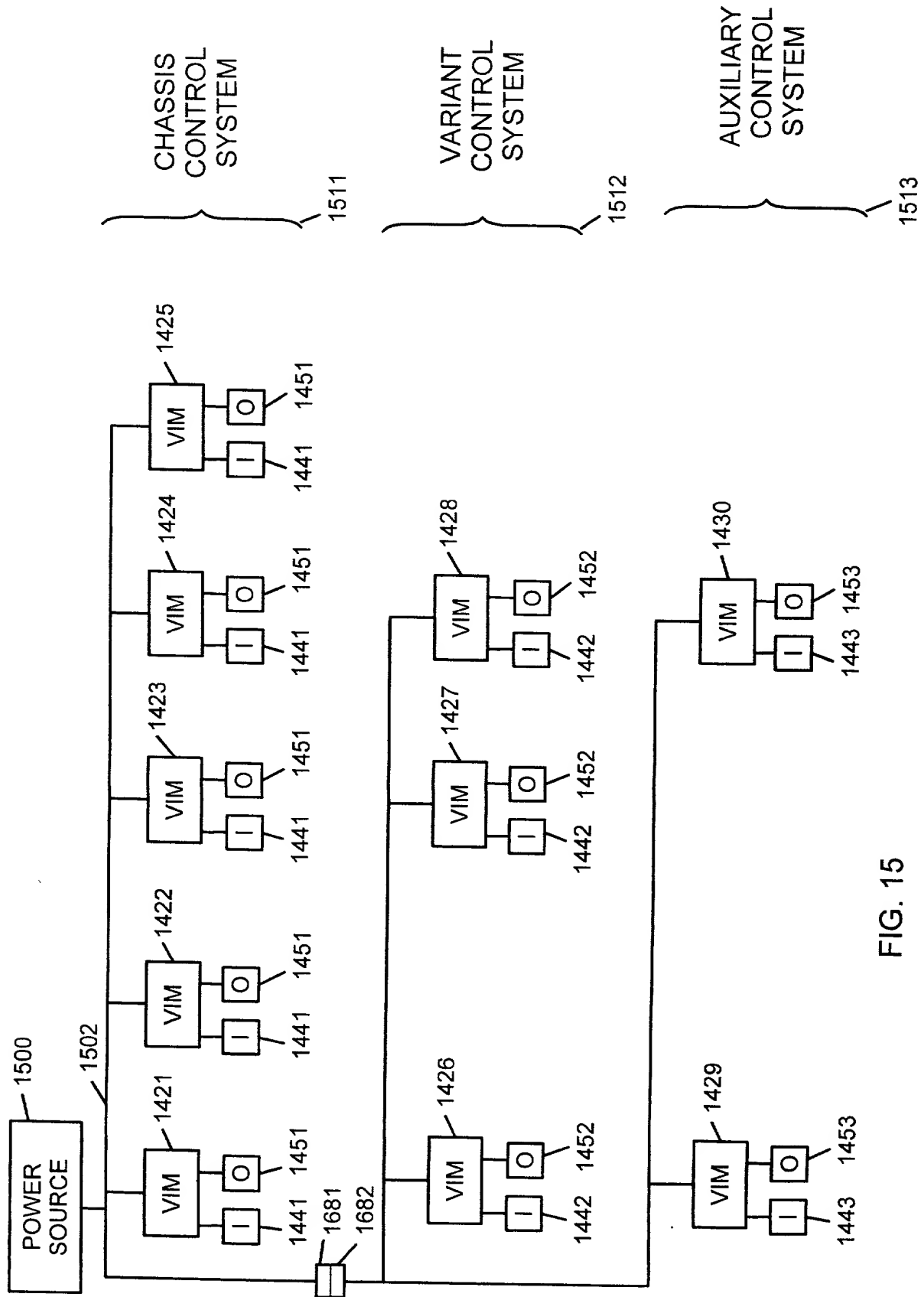


FIG. 15

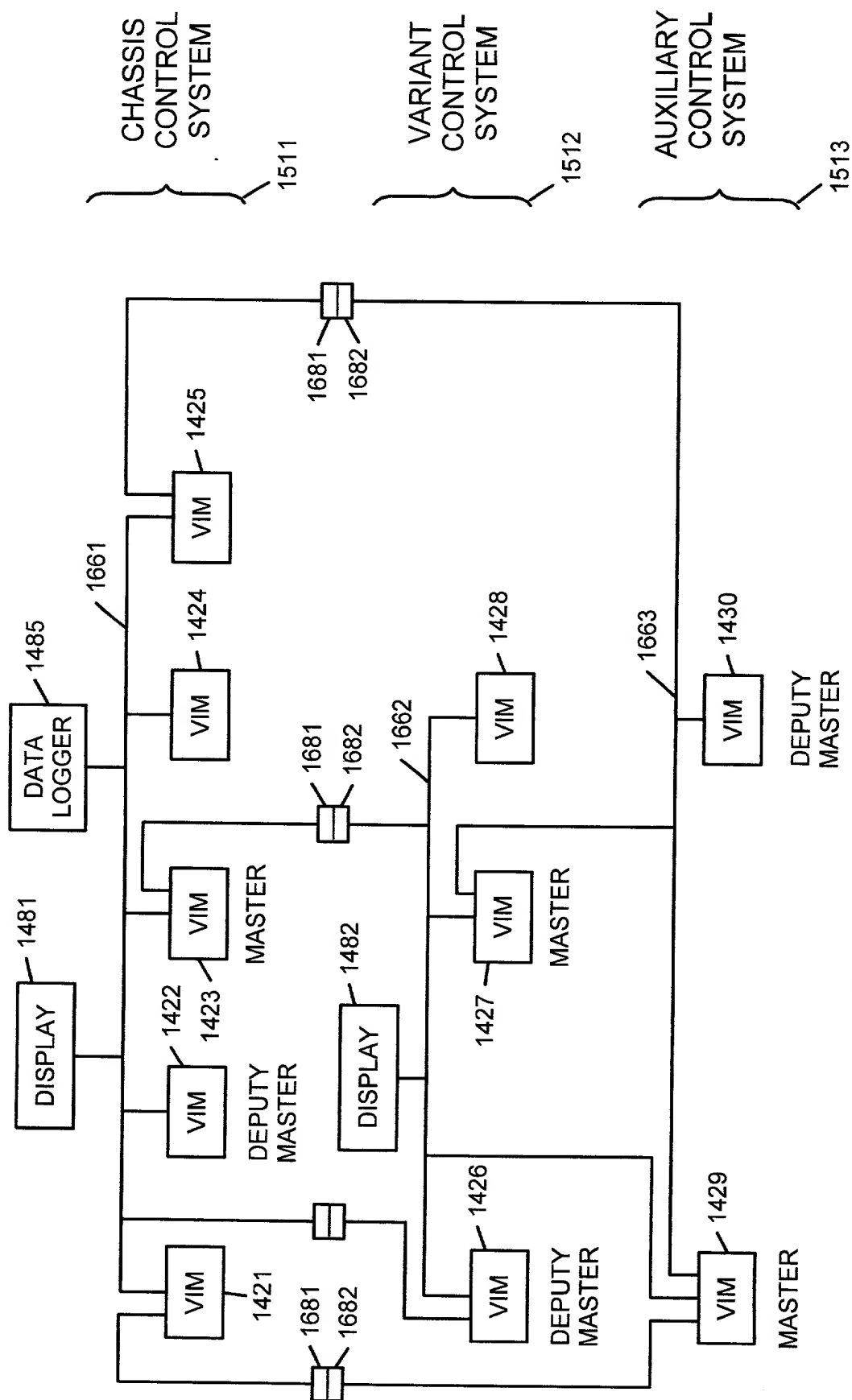


FIG. 16

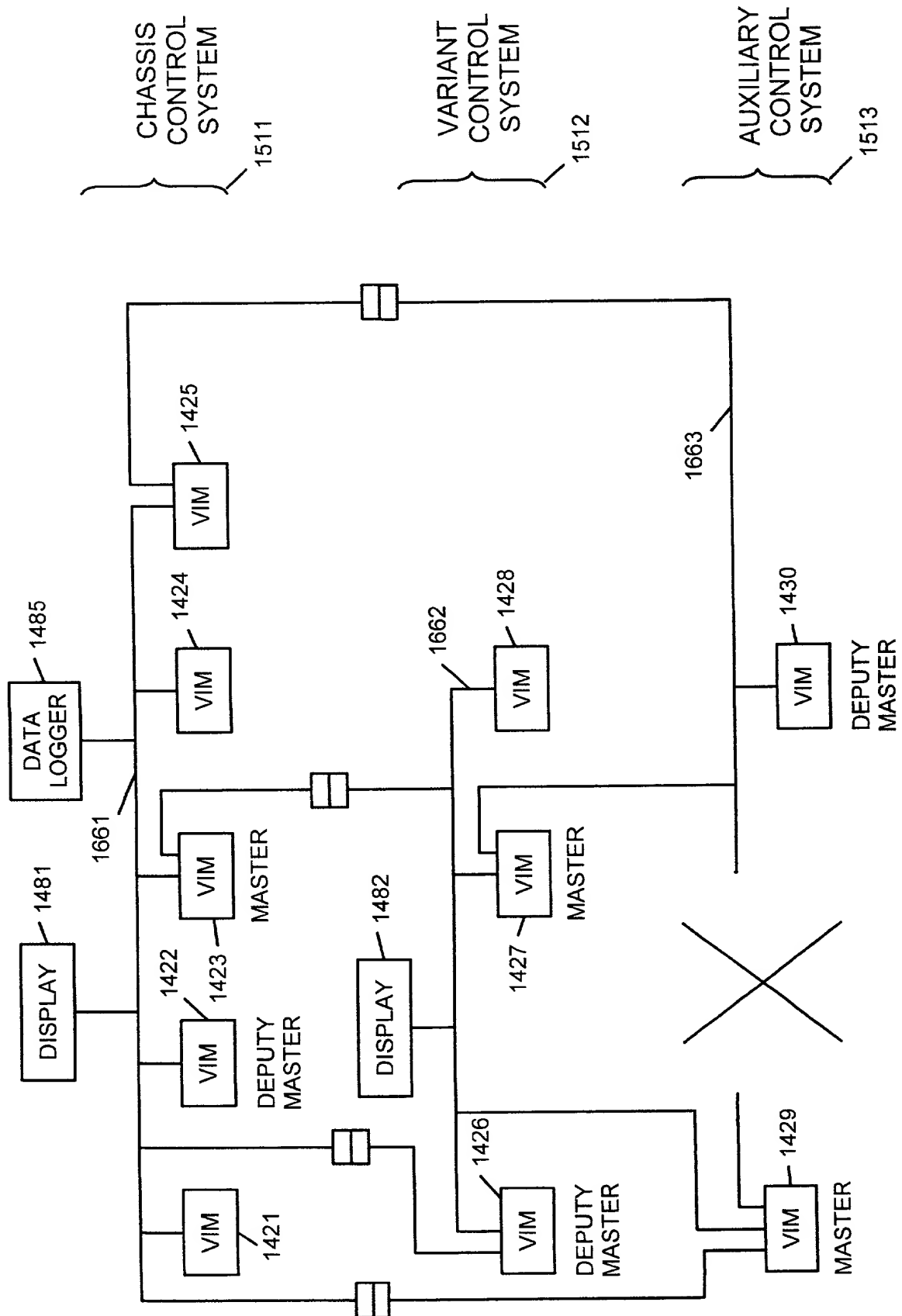


FIG. 17A

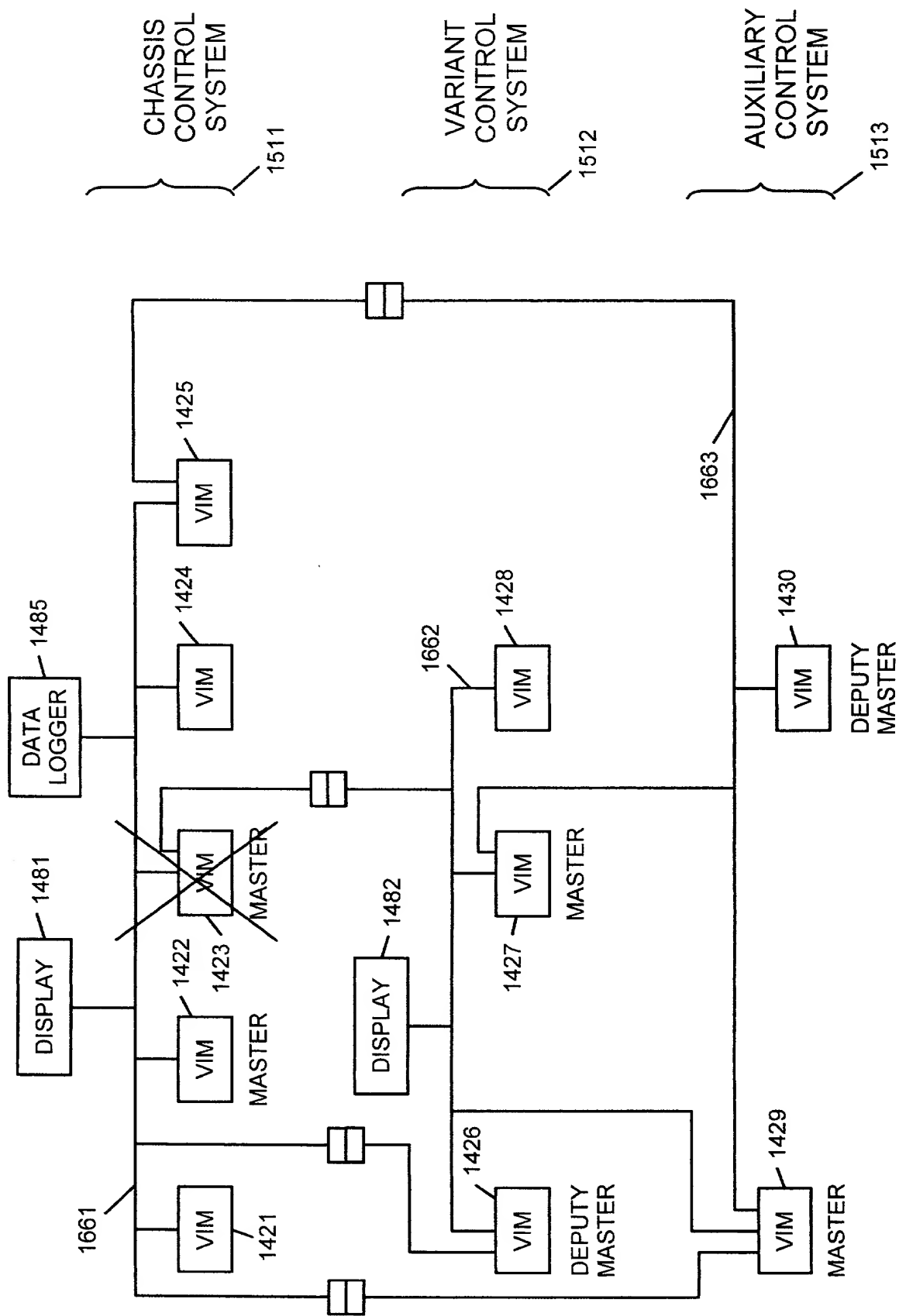


FIG. 17B

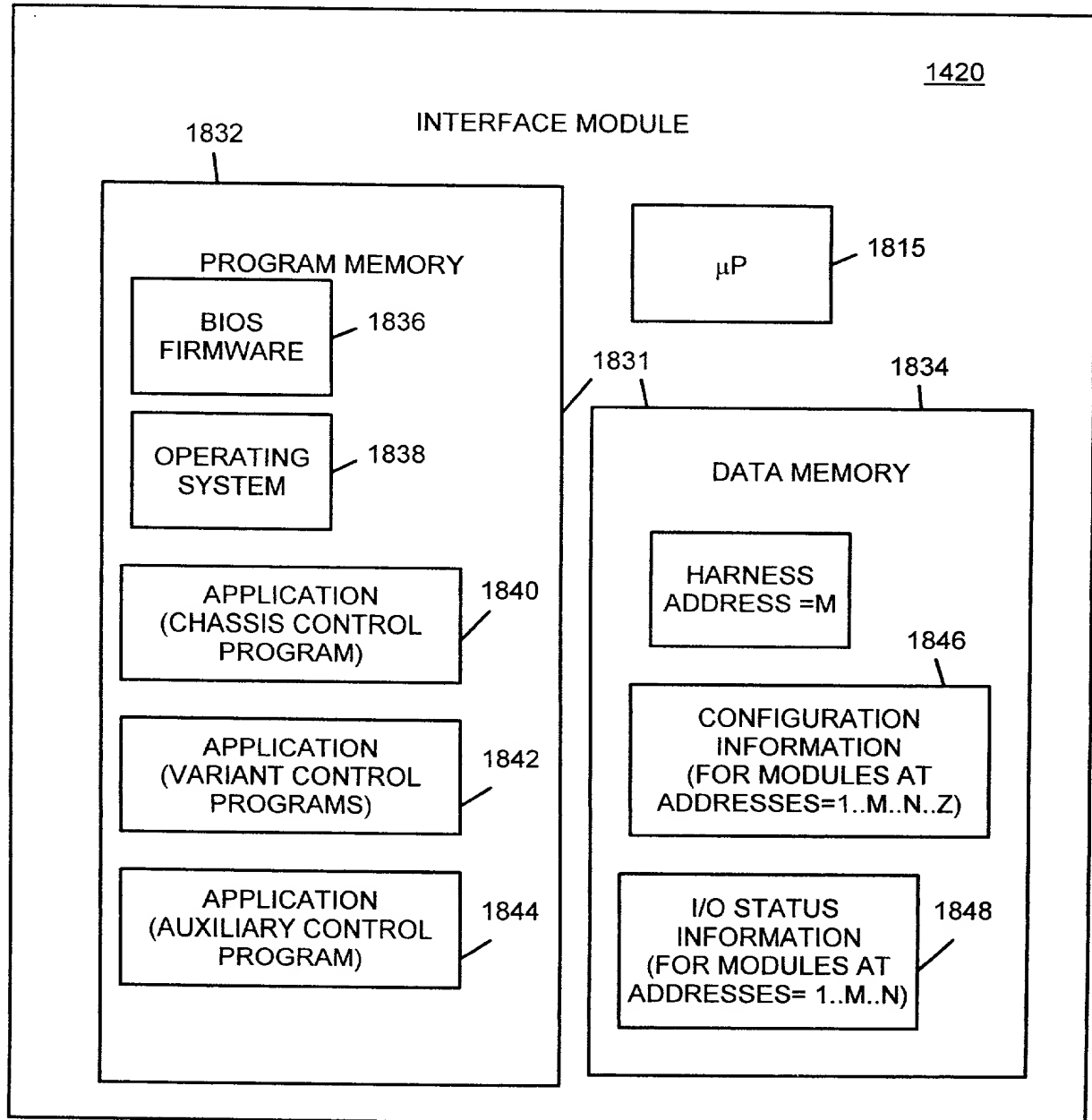
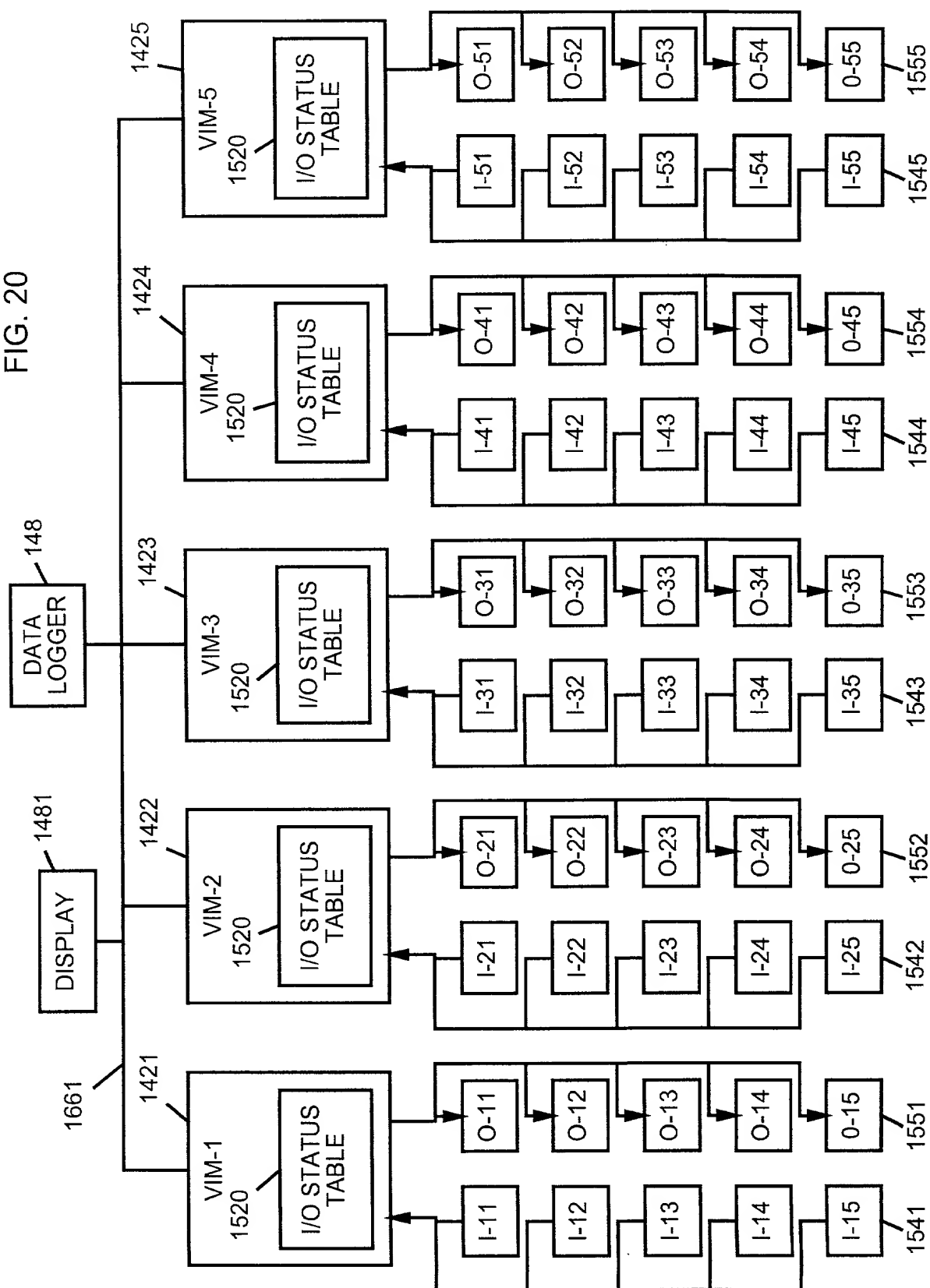


FIG. 18

STATE	INPUT #1	INPUT #2	OUTPUT #1	OUTPUT #2
1	OFF	OFF	OFF	OFF
2	OFF	ON	ON	ON
3	ON	OFF	OFF	OFF
4	ON	ON	OFF	OFF
5	OFF	?	ON	OFF
6	ON	?	OFF	OFF
7	?	ON	OFF	OFF
8	?	OFF	OFF	OFF
9	?	?	OFF	OFF

FIG. 19

FIG. 20



1520

I-11	I-12	I-13	I-14	I-15	IM-11	O-11	O-12	O-13
O-14	O-15	I-21	I-22	I-23	I-24	I-25	IM-21	IM-22
O-21	O-22	O-23	O-24	O-25	I-31	I-32	I-33	I-34
I-35	O-31	O-32	O-33	O-34	O-35	I-41	I-42	I-43
I-44	I-45	IM-41	O-41	O-42	O-43	O-44	O-45	I-51
I-52	I-53	I-54	I-55	O-51	O-52	O-53	O-54	O-55

FIG. 21

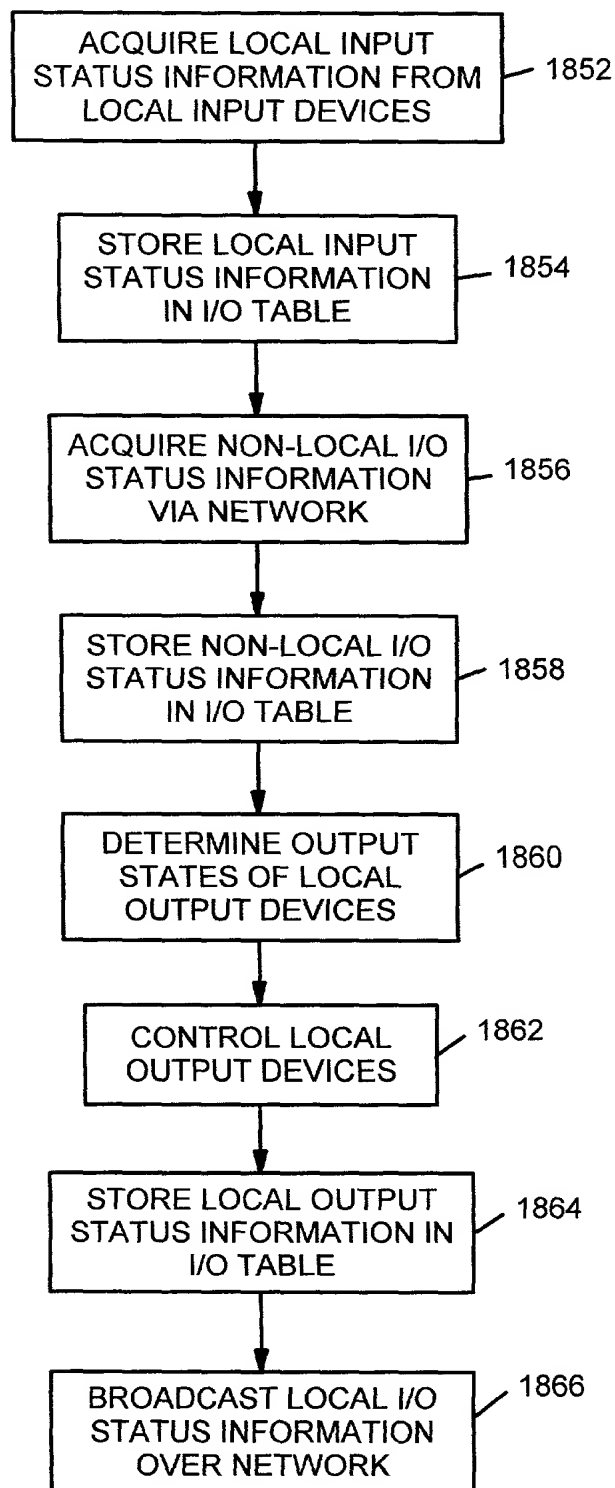


FIG. 22

FIG. 23

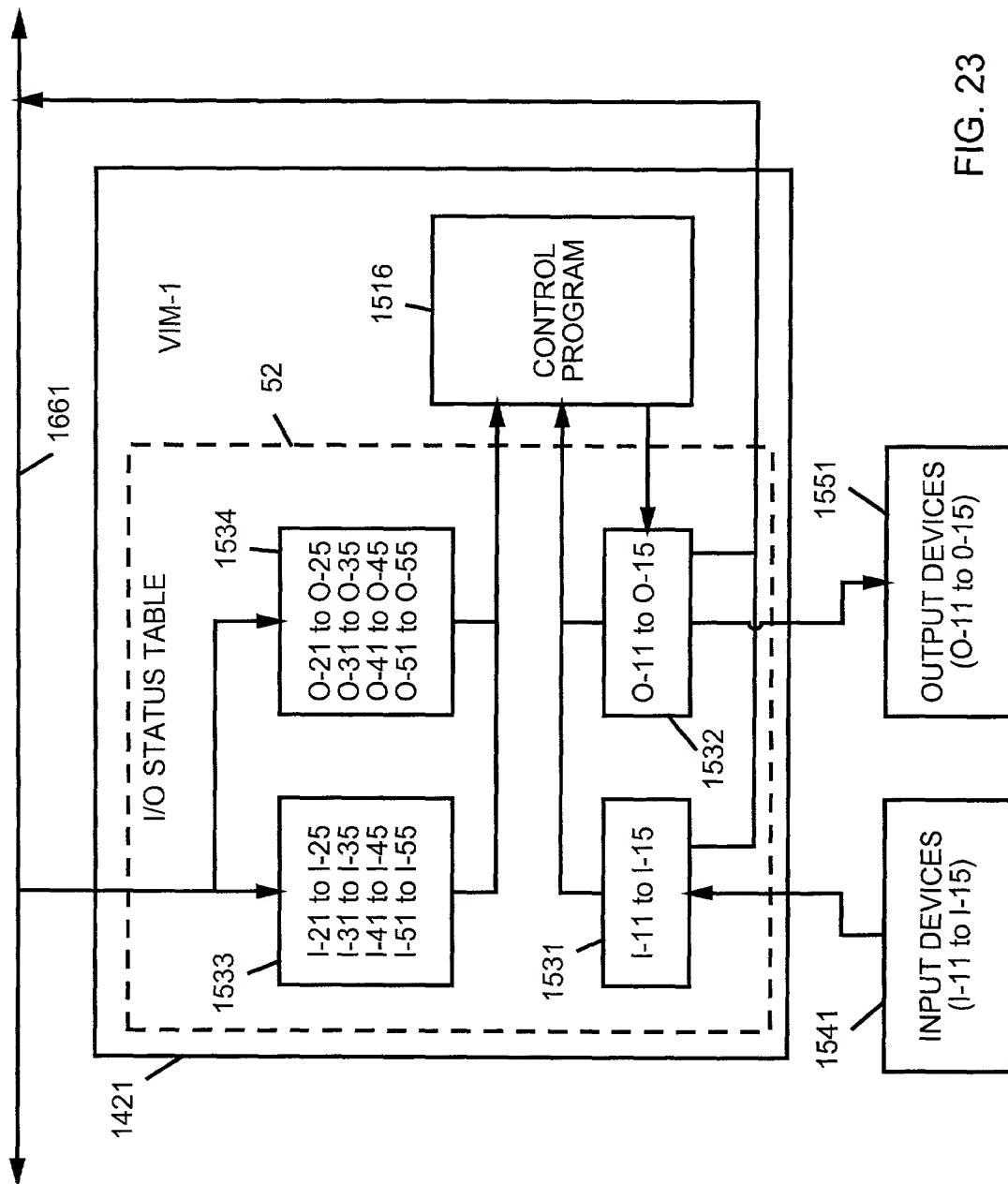


FIG. 23